REMARKS

This Amendment responds to the Office Action dated May 25, 2005 in which the Examiner rejected claims 1-3 and 5-6 under 35 U.S.C. §103.

As indicated above, claim 1 has been amended to incorporate information in the preamble into the body of the claim. Applicants respectfully submit that the amendment is unrelated to a statutory requirement for patentability and does not change the scope of the claim.

Claim 1 claims a delay time estimation method for estimating a delay time in a logic circuit that includes a MOS transistor. The method comprises the steps of: constructing a delay library including function information for specifying polygonal lines that provides a mode of an Ids-Vds characteristic at a given potential and also includes function information related to a slew rate specifying a fixed delay; modeling the MOS transistor by a resistive element having fixed resistance and a power source voltage that varies with time; and segmenting an operating characteristic of the MOS transistor thus modeled into a first region in which a current increases as a gate potential varies, a second region corresponding to a saturation region of the MOS transistor in which region the current gradually decreases as the gate potential remains constant, and a third region corresponding to a linearity region of the MOS transistor in which region the current decreases exponentially as the gate potential remains constant.

Through the method of the claimed invention, a) modeling an Ids-Vds characteristic by polygonal lines and b) constructing a delay library by functional information specifying the polygonal lines and functional information of a input slew rate, as claimed in claim 1, the claimed invention provides a delayed time estimation

method that matches the characteristics of the transistor. Furthermore, when the delay library is constructed as claimed, interpolation errors are reduced and the size of the library is reduced. The prior art does not show, teach or suggest the method as claimed in claim 1.

Claims 1-3 and 5 were rejected under 35 U.S.C. §103 as being unpatentable over *Arunachalum et al* (CMOS gate delay models for general RLC loading, IEEE 1997) in view of *Cocchini et al* (A comprehensive submicrometer MOST delay model and its application to CMOS buffers, August 1997). In addition, claim 4 was rejected under 35 U.S.C. §103 as being unpatentable over *Arunachalum et al* and *Cocchini et al* and further in view of *Iwanishi* (U.S. Patent No. 6,629,299).

Arunachalum et al appears to disclose a CMOS gate delay model for first computing the voltage wave-shape as a function of time and fitted by several ramps for several regions. In particular, a two-piece model shows excellent agreement with SPICE.

Thus, nothing in *Arunachalum et al* shows, teaches or suggests a) modeling an Ids-Vds characteristic by polygonal lines and b) constructing a delay library by functional information specifying polygonal lines and functional information of an input slew rate as claimed in claim 1. Rather, *Arunachalum et al* merely discloses using two segments.

Cocchini et al appears to disclose a delay model for MOS transistors including a region 0 when the transistor is off, a region 1 when M_1 is in saturation, while the input voltage is still increasing, a region 2 where M_1 is in saturation and V_T is constant, a region 4, where M_1 is in linearity and V_1 is stuck at V_{DD}.

Thus, nothing in *Cocchini et al* shows, teaches or suggests a) modeling an Ids-Vds characteristic by polygonal lines and b) constructing a delay library by functional information specifying polygonal lines and functional information of an input slew rate as claimed in claim 1. Rather, *Cocchini et al* merely discloses five regions, none of which is in a region which current decreases exponentially as the gate potential remains constant.

Since nothing in *Arunachalum et al*, or *Cocchini et al* shows, teaches or suggests a) modeling an Ids-Vds characteristic by polygonal lines and b) constructing a delay library by functional information specifying polygonal lines and functional information of an input slew rate as claimed in claim 1, applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claims 2-3 and 5-6 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 and 5-6 would not have been obvious within the meaning of 35 U.S.C. §103 over *Arunachalum et al* and *Cocchini et al* at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 and 5 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, applicants respectfully request the Examiner enters this Amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the

applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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